

SEMICONDUCTOR DEVICE AND MANUFACTURE THEREOF

Publication number: JP5003183

Publication date: 1993-01-08

Inventor: URUSHIMA MICHITAKA

Applicant: NIPPON ELECTRIC CO

Classification:

- international: H01L21/304; H01L21/321; H01L21/02; (IPC1-7):
H01L21/304; H01L21/321

- european:

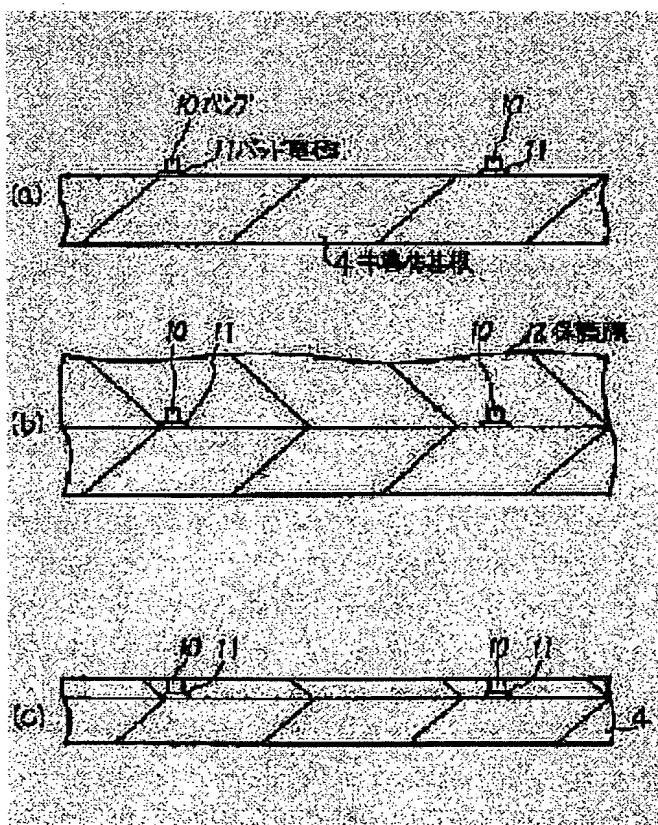
Application number: JP19910153650 19910626

Priority number(s): JP19910153650 19910626

Report a data error here

Abstract of JP5003183

PURPOSE:To enable a semiconductor substrate to be enhanced in mechanical strength and lessened in thickness by a method wherein a protective film is provided to the semiconductor substrate to cover its surface including the side faces of bumps provided to pad electrodes, and the upside of the protective film is set level with those of the bumps so as to enable the upsides of the bumps to be exposed. **CONSTITUTION:**Pad electrodes 11 electrically connected to the outside are provided onto a semiconductor substrate 4 where semiconductor elements are formed, a metal film of Ti or the like is formed on the surface of the substrate 4 including the pad electrodes 11, the pad electrodes 11 are selectively plated with Au or the like making the metal film serve as a plating electrode, then the metal film is removed, and bumps 10 are formed. Then, a protective film 12 of epoxy resin or the like is applied onto all the surface of the substrate 4 including the bumps 10 as thick as 200 μ m and then cured. In succession, the semiconductor substrate 4 is rendered as thin as 200 μ m or so by grinding its rear side, and furthermore the protective film 12 is etched back to be as thin as 20 μ m or so to make the upsides of the bumps 10 exposed.



Data supplied from the **esp@cenet** database - Worldwide

Best Available Copy

【特許請求の範囲】

【請求項1】 半導体基板上に設けたパッド電極と、前記パッド電極上に設けたバンプと、前記バンプの側面を含む表面を被覆し且つ上面を前記バンプの上面と同一平面として前記バンプの上面を露出させた保護膜とを有することを特徴とする半導体装置。

【請求項2】 半導体基板の厚さが保護膜の厚さより薄い請求項1記載の半導体装置。

【請求項3】 半導体素子を設けた半導体基板上に外部接続用のパッド電極を設け前記パッド電極上に金属層を選択的に堆積してバンプを形成する工程と、前記バンプを含む表面に保護膜を形成する工程と、前記半導体基板の裏面を研削して前記半導体基板の厚さを薄くする工程と、前記保護膜を研削して前記バンプの上面を露出させる工程とを含むことを特徴とする半導体装置の製造方法。

【発明の詳細な説明】

【0001】

【産業上の利用分野】 本発明は半導体装置及びその製造方法に関する。

【0002】

【従来の技術】 従来の半導体装置の製造方法は、まず、図3(a)に示すように、半導体素子が形成された半導体基板4の上に外部との電気的接続行なうためのパッド電極11を選択的に形成する。

【0003】 次に、図3(b)に示すように、パッド電極11を含む半導体基板4の表面にTi, Cr, Cu等の金属膜14を堆積した後、フォトリソグラフィ技術及びめっき法を用いてパッド電極11上の金属膜14の上に選択的に、Au, Cu, Pb-Sn等のバンプ10を形成する。

【0004】 次に、図3(c)に示すように、バンプ10をマスクとして金属膜14をエッチング除去して半導体装置を構成していた。

【0005】 このようなバンプを有する半導体装置を実装する方法の一つにフリップチップがある。これは図4(a)に示すように、実装基板15のボンディングパッド13とPb-Sn等からなる、バンプ10とを半田熔融することにより接続する。次いで、半導体素子の保護のために、エポキシ樹脂等の樹脂層17で被覆する。

【0006】 また、同様にバンプを有する半導体基板4を実装する方法として、フィルムキャリア方式がある。これは、図4(b)に示すように、バンプ10と、フィルムキャリアテープ上のインナーリード6を熱圧着法又は共晶法を用いて接続(Inner Lead Bonding)する。次に、半導体基板4表面に信頼性の向上及び機械的保護を目的として、例えば、エポキシ樹脂等の樹脂層17を滴下して、半導体チップ表面を樹脂封止する。次いで、電気選別用パッド9を用いて電気検査及びバーンインテストを行なう。さらに、実装基板に実

2

装する場合は、所定寸法にアウターリード7を切断し、成形した後、実装基板15のボンディングパッド13とアウターリード7とをボンディングして実装する。

【0007】

【発明が解決しようとする課題】 上述した半導体装置は、フリップチップ方式の実装後半導体素子の保護として形成する樹脂層が実装基板と半導体基板の間に完全に充填するのが非常にむずかしく、さらにこれを確認することが難しい。又、従来の半導体装置は半導体基板の厚さが500 μ m、樹脂層の厚さが100~300 μ mで、全体として600~800 μ mの厚さを有している。電子装置の軽量化・薄型化に伴って、これらの半導体装置の更なる薄型化が要求されている。すなわち、800 μ m程度の厚さをさらに薄くする必要がある。そのために、半導体基板を研削する方法があるが、割れ等の破損に至ることが多い。また樹脂厚についても、半導体素子表面を完全に被覆するためには、ある一定量の樹脂を滴下する必要があり薄型化に限界があった。

【0008】

【課題を解決するための手段】 本発明の半導体装置は、半導体基板上に設けたパッド電極と、前記パッド電極上に設けたバンプと、前記バンプの側面を含む表面を被覆し且つ上面を前記バンプの上面と同一平面として前記バンプの上面を露出させた保護膜とを有する。

【0009】 本発明の半導体装置の製造方法は、半導体素子を設けた半導体基板上に外部接続用のパッド電極を設け前記パッド電極上に金属層を選択的に堆積してバンプを形成する工程と、前記バンプを含む表面に保護膜を形成する工程と、前記半導体基板の裏面を研削して前記半導体基板の厚さを薄くする工程と、前記保護膜を研削して前記バンプの上面を露出させる工程とを含んで構成される。

【0010】

【実施例】 次に、本発明について図面を参照して説明する。

【0011】 図1(a)~(c)は、本発明の一実施例の製造方法を説明するための工程順に示した半導体チップの断面図である。

【0012】 まず、図1(a)に示すように、従来例と同様の工程により半導体素子を形成した半導体基板4上に、外部との電気的接続を行なうためのパッド電極11を形成し、パッド電極11を含む表面に例えば、Ti, Cr, Cu等の金属膜(図示せず)を形成し、次いで、金属膜をめっき電極として選択的にパッド電極11上に例えばAu, Cu, Pb-Sn等をめっきした後金属膜を除去してバンプ10を形成する。なお、このバンプ形成は、めっき法の他に、特開昭49-52973号公報に記載されているように、Au, Pb-Sn等からなるワイヤーをワイヤーボンディング法を使用して、ボール形成し、ボールをパッド上に接合後ボールのみを残し、

3

ワイヤーを切断することによってバンパを形成する方法や、熔融半田中に浸漬してパッド電極上のみに半田バンパを形成する方法等の従来のバンパ形成法を利用することができる。

【0013】次に、図1 (b) に示ように、バンパ10を含む半導体基板4上全面に、例えばエポキシ樹脂等の保護膜12を200 μ mの厚さに塗布し、硬化させる。

【0014】次に図1 (c) に示すように、半導体基板4の裏面を研削して半導体基板の厚さを200 μ m程度まで薄くし、さらに保護膜12を樹脂厚が20 μ m程度になるまでエッチバックしてバンパ10の上面を露出させる。なお、半導体基板4の放熱性を考慮して、あらかじめ、ボールバンパを2重、3重に形成する等によりバンパ10の高さを高くしておき、強度を保ために、樹脂厚を100 μ m程度に厚くし、半導体基板4を50 μ m程度に薄くしていても良い。

【0015】図2 (a) , (b) は本発明の半導体装置の実装状態を示す断面図である。

【0016】図2 (a) はフリップチップ法による実装例で、露出したバンパ10上又は、実装基板15のボンディングパッド13上に設けた第2のバンパ16を介して半導体装置を実装する。

【0017】ここで、バンパ16の形成法は、半導体基板上にバンパを形成した場合と同様に、めっき法、ボールバンパ法があるが、その他に、「日経マイクロデバイス」1989年、7月号、43～65頁に記載されているように、Auバンパの上にAgペースト等の導電性ペーストを更に塗布する方法や、導電性樹脂を印刷や滴下法により形成する方法等があり、従来のバンパ形成法を利用して、容易に実施できる。また、バンパの代りに微小なピンやリードを用いることもできる。次に、接続の方法、例えば、露出バンパ10と第2のバンパ16の組み合わせが、半田-半田の場合は、熔融によって接続し、Au-Auの場合は、異方導電性シートを用いて接続し、導電性接着剤の場合は、硬化によって接続する等バンパ材料により適切な接続方法を選択する。

【0018】図2 (b) は、フィルムキャリアテープを利用した実装例で、保護膜12に露出したバンパ10上又は、インナーリード部に第2のバンパ16を形成し、

4

インナーリードボンディングを例えば熱圧着法等で実施する。次いで、実装基板15上のボンディングパッド13でアウターリード部7と、アウターリードボンディングを例えば、熱圧着法で実施する。なおバンパ16の形成方法は、フリップチップの場合と同様に行なう。更に、バンパ16を形成せずに直接リードを露出したバンパ10にボンディングすることも可能である。また、露出したバンパ10の上に直接ワイヤーボンディングすることにより、従来のワイヤーボンディング半導体装置用の半導体基板としても、利用することができる。

【0019】

【発明の効果】以上説明したように本発明は、半導体基板厚を、従来に比べ、さらに薄くすることが可能となるため、薄型及び軽量の半導体装置の製造が可能となる。又、保護樹脂の形成が容易でかつ、薄くできる。さらに従来のフリップチップ法で実装後、実装基板全面に樹脂を被覆する場合は、基板実装後不良発生時の個別単位の交換が困難であったが、本発明では、個別に、樹脂封止及び実装できることから、個別単位の交換が可能という効果も有する。

【図面の簡単な説明】

【図1】本発明の一実施例の製造方法を説明するための工程順に示した半導体チップの断面図。

【図2】本発明の半導体装置の実装状態を示す断面図。

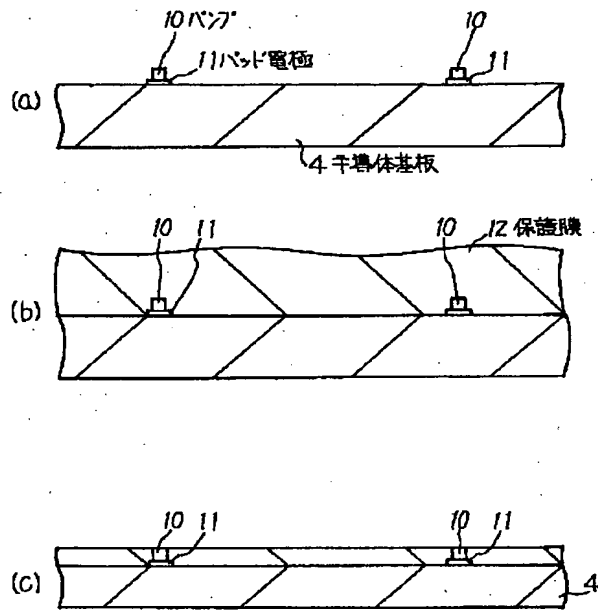
【図3】従来の半導体装置の製造方法を説明するための工程順に示した半導体チップの断面図。

【図4】従来の半導体装置の実装状態を示す断面図。

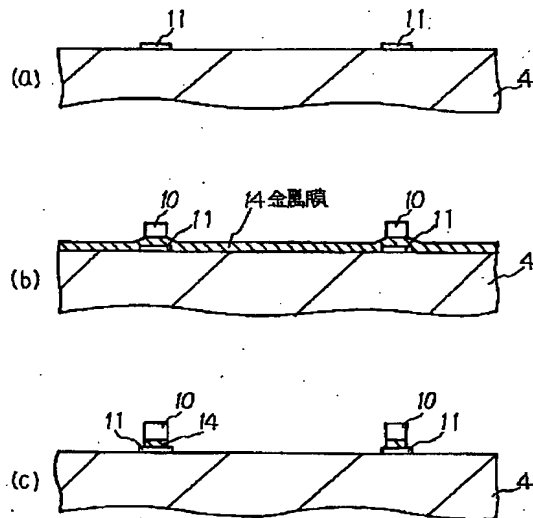
【符号の説明】

- 4 半導体基板
- 6 インナーリード
- 7 アウターリード
- 10, 16 バンパ
- 11 パッド電極
- 12 保護膜
- 13 ボンディングパッド
- 14 金属膜
- 15 実装基板
- 17 樹脂層

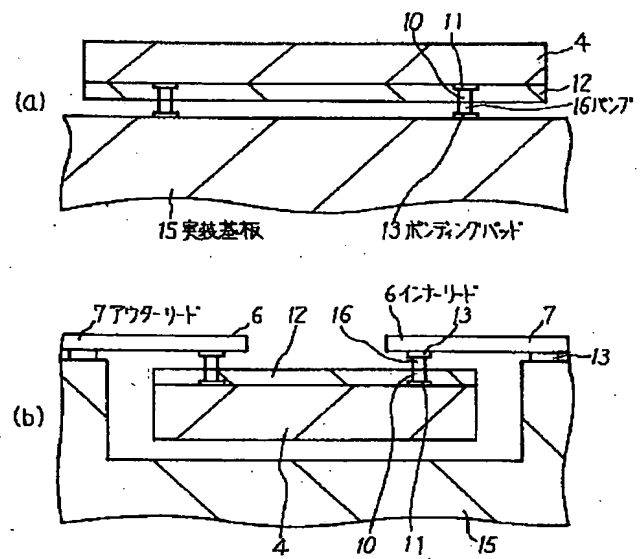
【図 1】



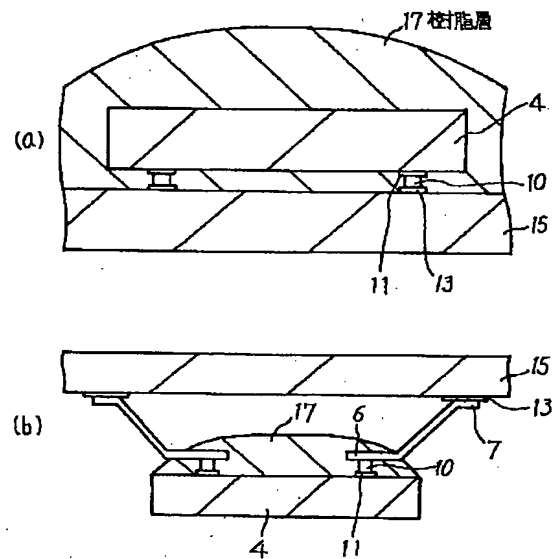
【図 3】



【図 2】



【図 4】



(19)日本国特許庁 (J P)

(12) 公 開 特 許 公 報 (A)

(11)特許出願公開番号

特開平5-3183

(43)公開日 平成5年(1993)1月8日

(51)Int.Cl.⁵

H 0 1 L 21/304
21/321

識別記号

3 2 1 B

庁内整理番号

8831-4M

9168-4M

F I

H 0 1 L 21/ 92

技術表示箇所

F

審査請求 未請求 請求項の数3(全 4 頁)

(21)出願番号

特願平3-153650

(22)出願日

平成3年(1991)6月26日

(71)出願人 000004237

日本電気株式会社

東京都港区芝五丁目7番1号

(72)発明者 漆島 路高

東京都港区芝五丁目7番1号日本電気株式
会社内

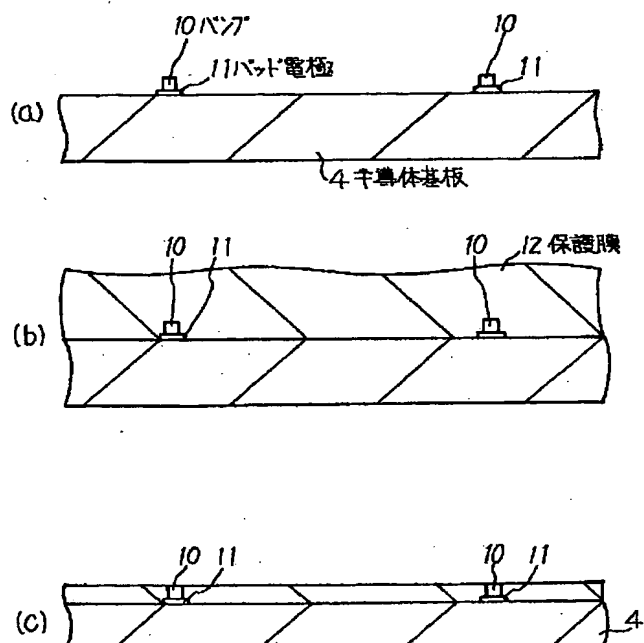
(74)代理人 弁理士 内原 晋

(54)【発明の名称】 半導体装置及びその製造方法

(57)【要約】

【構成】半導体基板4の上に設けたパッド電極11の上にバンプ10を形成し、保護膜12を塗布して硬化後、半導体基板4の裏面を研削し、次に、保護膜12をバンプ10が露出するまで研削する。

【効果】保護膜の形成により、半導体基板の機械的強度を補強して半導体基板の厚さを薄くでき、実装状態の厚さを薄くできる。



PATENT ABSTRACTS OF JAPAN

(11)Publication number : 05-003183

(43)Date of publication of application : 08.01.1993

(51)Int.Cl.

H01L 21/304
H01L 21/321

(21)Application number : 03-153650

(71)Applicant : NEC CORP

(22)Date of filing : 26.06.1991

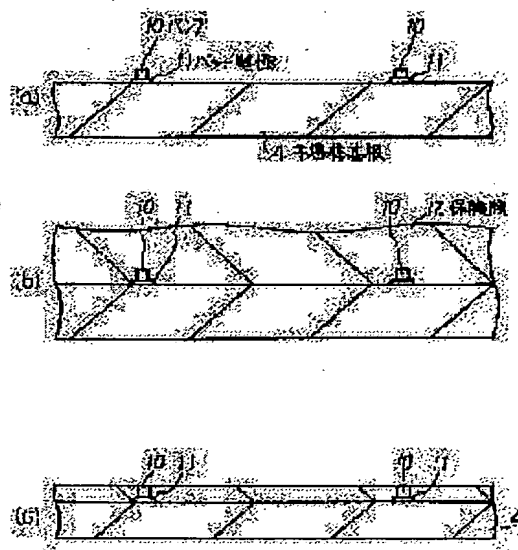
(72)Inventor : URUSHIMA MICHITAKA

(54) SEMICONDUCTOR DEVICE AND MANUFACTURE THEREOF

(57)Abstract:

PURPOSE: To enable a semiconductor substrate to be enhanced in mechanical strength and lessened in thickness by a method wherein a protective film is provided to the semiconductor substrate to cover its surface including the side faces of bumps provided to pad electrodes, and the upside of the protective film is set level with those of the bumps so as to enable the upsides of the bumps to be exposed.

CONSTITUTION: Pad electrodes 11 electrically connected to the outside are provided onto a semiconductor substrate 4 where semiconductor elements are formed, a metal film of Ti or the like is formed on the surface of the substrate 4 including the pad electrodes 11, the pad electrodes 11 are selectively plated with Au or the like making the metal film serve as a plating electrode, then the metal film is removed, and bumps 10 are formed. Then, a protective film 12 of epoxy resin or the like is applied onto all the surface of the substrate 4 including the bumps 10 as thick as 200 μ m and then cured. In succession, the semiconductor substrate 4 is rendered as thin as 200 μ m or so by grinding its rear side, and furthermore the protective film 12 is etched back to be as thin as 20 μ m or so to make the upsides of the bumps 10 exposed.



LEGAL STATUS

[Date of request for examination]

30.06.1995

[Date of sending the examiner's decision of rejection]

[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]

[Date of final disposal for application]

[Patent number]

2701589

[Date of registration]

03.10.1997

[Number of appeal against examiner's decision of rejection]

[Date of requesting appeal against examiner's decision of rejection]

[Date of extinction of right]

NOTICES *

PO and NCIP are not responsible for any damages caused by the use of this translation.

.This document has been translated by computer. So the translation may not reflect the original precisely.
**** shows the word which can not be translated.
In the drawings, any words are not translated.

CLAIMS

Claim(s)]

Claim 1] The semiconductor device characterized by having the protective coat to which the front face including the side face of the pad electrode prepared on the semi-conductor substrate, the bump who prepared on said pad electrode, and said bump was covered, and said bump's top face was exposed for the top face as the same flat surface as said bump's top face.

Claim 2] A semiconductor device according to claim 1 with the thickness of a semi-conductor substrate thinner than the thickness of a protective coat.

Claim 3] The process which prepares the pad electrode for external connection on the semi-conductor substrate which prepared the semiconductor device, deposits a metal layer alternatively on said pad electrode, and forms a bump, The manufacture approach of the semiconductor device characterized by including the process which forms a protective coat in a front face including said bump, the process which carries out grinding of the rear face of said semi-conductor substrate, and makes thickness of said semi-conductor substrate thin, and the process at which grinding of said protective coat is carried out, and said bump's top face is exposed.

[Translation done.]

NOTICES *

PO and NCIP are not responsible for any damages caused by the use of this translation.

.This document has been translated by computer. So the translation may not reflect the original precisely.
**** shows the word which can not be translated.
.In the drawings, any words are not translated.

DETAILED DESCRIPTION

Detailed Description of the Invention]

[0001]

Industrial Application] This invention relates to a semiconductor device and its manufacture approach.

[0002]

Description of the Prior Art] the semi-conductor substrate 4 top with which the semiconductor device was formed as the manufacture approach of the conventional semiconductor device was first shown in drawing 3 (a) -- an electric connecting row with the exterior -- ** -- it obtains and the pad electrode 11 of a sake is formed alternatively.

[0003] Next, as shown in drawing 3 (b), after depositing the metal membranes 14, such as Ti, Cr, and Cu, on the front face of the semi-conductor substrate 4 containing the pad electrode 11, the bumps 10, such as Au, Cu, and Pb-Sn, are alternatively formed on the metal membrane 14 on the pad electrode 11 using a photolithography technique and the galvanizing method.

[0004] Next, as shown in drawing 3 (c), etching removal of the metal membrane 14 was carried out by having used the bump 10 as the mask, and the semiconductor device was constituted.

[0005] A flip chip is in one of the approaches which mounts the semiconductor device which has such a bump. This is connected by carrying out solder fusion of the bump 10 who consists of a bonding pad 13, Pb-Sn, etc. of the mounting substrate 15, as shown in drawing 4 (a). Subsequently, it covers with the resin layers 17, such as an epoxy resin, for protection of a semiconductor device.

[0006] Moreover, there is a tape carrier package method as an approach of mounting the semi-conductor substrate 4 which has a bump similarly. This connects the inner lead 6 on a tape carrier package tape with a bump 10 using thermocompression bonding or an eutectic method, as shown in drawing 4 (b) (Inner Lead Bonding). Next, the resin layers 17, such as an epoxy resin, are dropped at semi-conductor substrate 4 front face for the purpose of the improvement in dependability, and mechanical protection, for example, the resin seal of the semiconductor chip front face is carried out. Subsequently, an electric inspection and a burn-in test are performed using the pad 9 for electric sorting. Furthermore, when it mounts in a mounting substrate, after cutting and fabricating an outer lead 7 in a predetermined dimension, bonding of the bonding pad 13 and outer lead 7 of the mounting substrate 15 is carried out, and they are mounted.

[0007]

[Problem(s) to be Solved by the Invention] It is very difficult for the semiconductor device mentioned above for the resin layer formed as protection of a conductive element in the mounting second half of a flip chip method to be completely filled up between a mounting substrate and a semi-conductor substrate, and it is difficult for it to check this further. Moreover, the thickness of 500 micrometers and a resin layer is 100-300 micrometers, and, as for the conventional semiconductor device, the thickness of a semi-conductor substrate has the thickness of 600-800 micrometers as a whole. The further thin shape-ization of a coming [it] semiconductor device is demanded with lightweight-izing and thin-shape-izing of an electronic instrument. That is, it is necessary to make thickness of about 800 micrometers still thinner. Therefore, although there is the approach of carrying out grinding of the semi-conductor substrate, it results in breakage of a crack etc. in many cases. Moreover, also about resin thickness, in order to cover a semiconductor device front face completely, the resin of a certain constant rate needed to be dropped and the limitation was in thin shape-ization.

[0008]

[Means for Solving the Problem] The semiconductor device of this invention has the protective coat to which the front face including the side face of the pad electrode prepared on the semi-conductor substrate, the bump who prepared on said pad electrode, and said bump was covered, and said bump's top face was exposed for the top face as the same flat surface as said bump's top face.

[0009] The process which the manufacture approach of the semiconductor device of this invention prepares the pad electrode for external connection on the semi-conductor substrate which prepared the semiconductor device, deposits a metal layer alternatively on said pad electrode, and forms a bump. It is constituted including the process which forms a protective coat in a front face including said bump, the process which carries out

grinding of the rear face of said semi-conductor substrate, and makes thickness of said semi-conductor substrate thin, and the process at which grinding of said protective coat is carried out, and said bump's top face is exposed.

[0010]

Example] Next, this invention is explained with reference to a drawing.

[0011] Drawing 1 (a) - (c) is the sectional view of the semiconductor chip shown in order of the process for explaining the manufacture approach of one example of this invention.

[0012] As shown in drawing 1 (a), on the front face which forms the pad electrode 11 for performing electrical installation with the exterior on the semi-conductor substrate 4 which formed the semiconductor device according to the same process as the conventional example, and contains the pad electrode 11 first, for example metal membranes (not shown), such as Ti, Cr, and Cu, are formed, subsequently to the pad electrode 11 top, a metal membrane is removed and a bump 10 is formed, after galvanizing a metal membrane for Au, Cu, Pb-Sn, etc. alternatively as a plating electrode. In addition, this bump formation as indicated by JP,49-52973, A other than the galvanizing method The wire-bonding method is used for the wire which consists of Au, Pb-Sn, etc. Ball formation can be carried out, it can leave only the ball after junction for a ball on a pad, and the conventional bump forming methods, such as the approach of forming a bump and an approach which is immersed into melting solder and forms a solder bump only on a pad electrode, can be used by cutting a wire.

[0013] Next, the protective coats 12, such as EPOKIN resin, are applied to the thickness of 200 micrometers, and drawing 1 (b) is made to harden them like all over the ** substrate [semi-conductor] 4 top including a bump 10.

[0014] Next, as shown in drawing 1 (c), grinding of the rear face of the semi-conductor substrate 4 is carried out, thickness of a semi-conductor substrate is made thin to about 200 micrometers, further, etchback of the protective coat 12 is carried out until resin thickness is set to about 20 micrometers, and a bump's 10 top face is exposed. In addition, in consideration of the heat dissipation nature of the semi-conductor substrate 4, a bump's 10 height is beforehand made high by forming a ball bump in three-fold [a duplex and] etc., resin thickness may be made thick to about 100 micrometers for reinforcement at a ** sake, and the semi-conductor substrate 4 may be made thin at about 50 micrometers.

[0015] Drawing 2 (a) and (b) are the sectional views showing the mounting condition of the semiconductor device of this invention.

[0016] Drawing 2 (a) is an example of mounting by the flip chip method, and mounts a semiconductor device through the 2nd bump 16 who prepared on the bump 10 who exposed, or the bonding pad 13 of the mounting substrate 15.

[0017] Although a bump's 16 method of forming has the galvanizing method and the ball bump method like the case where a bump is formed on a semi-conductor substrate here In addition, as indicated by the "Nikkei micro device" July, 1989 issue and 43-65 pages There are an approach of applying conductive pastes, such as Ag paste, further on Au bump, the approach of forming conductive resin with printing or a dropping test, etc., and it can carry out easily using the conventional bump forming method. Moreover, pin minute instead of and lead minute instead of of a bump can also be used. Next, in the case of solder-solder, the approach of connection, for example, the combination of the exposure bump 10 and the 2nd bump 16, connects by melting, in Au-Au, it connects using an anisotropic conductive sheet, and, in the case of electroconductive glue, a suitable connection method is chosen with a bump ingredient, such as connecting by hardening.

[0018] Drawing 2 (b) is an example of mounting using a tape carrier package tape, forms the 2nd bump 16 in the bump 10 top who exposed to the protective coat 12, or the inner lead section, and carries out inner lead bonding by thermocompression bonding etc. Subsequently, outer lead bonding is carried out by thermocompression bonding with the outer lead section 7 with the bonding pad 13 on the mounting substrate 15. In addition, a bump's 16 formation approach is performed like the case of a flip chip. Furthermore, it is also possible to carry out bonding to the bump 10 who exposed the direct lead, without forming a bump 16. Moreover, it can use also as a semi-conductor substrate for the conventional wire-bonding semiconductor devices by carrying out direct wire bonding on the bump 10 who exposed.

[0019]

[Effect of the Invention] As explained above, since this invention becomes possible [making semi-conductor substrate thickness still thinner compared with the former], the manufacture of the semiconductor device of a thin shape and a lightweight mold of it is attained. Moreover, formation of protection resin can be performed easily thinly. When covering resin with the further conventional flip chip method all over a mounting substrate after mounting, exchange of the individual unit at the time of poor after [substrate mounting] generating was difficult, but in this invention, according to an individual, a resin seal and since it can mount, it also has the effectiveness that exchange of an individual unit is possible.

: NOTICES *

PO and NCIP are not responsible for any
damages caused by the use of this translation.

.This document has been translated by computer. So the translation may not reflect the original precisely.
!**** shows the word which can not be translated.
!.In the drawings, any words are not translated.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

Drawing 1] The sectional view of the semiconductor chip shown in order of the process for explaining the manufacture approach of one example of this invention.

Drawing 2] The sectional view showing the mounting condition of the semiconductor device of this invention.

Drawing 3] The sectional view of the semiconductor chip shown in order of the process for explaining the manufacture approach of the conventional semiconductor device.

Drawing 4] The sectional view showing the mounting condition of the conventional semiconductor device.

[Description of Notations]

! Semi-conductor Substrate

;) Inner Lead

7 Outer Lead

10 16 Bump

11 Pad Electrode

12 Protective Coat

13 Bonding Pad

14 Metal Membrane

15 Mounting Substrate

17 Resin Layer

[Translation done.]